JSS Mahavidyapeetha
JSS Academy of Technical Education, Bengaluru
Department of Electronics & Communication Engineering

FACULTY PROFILE

1. Personal Details

NAME	Dr. Poornima N
DEPARTMENT	Electronics & Communication Engineering
DESIGNATION	Associate Professor
PHONE	**9845988280**
EMAIL ID	**poorniman@jssateb.ac.in**
TEACHING EXPERIENCE	**22.5 Years**
INDUSTRY EXPERIENCE	**--**
RESEARCH EXPERIENCE	**10 Years**

2. Qualification

COURSES	SPECIALIZATION	INSTITUTION	UNIVERSITY
PhD	Low Power VLSI Design	VIT University, Chennai Tamilnadu	VIT University, Chennai Tamilnadu
Mtech	VLSI Design and Embedded Systems	BMS College of Engineering Bangalore Karnataka, INDIA	Visvesvaraya Technological University , Belgavi,Karnataka
BE	Electronics and Communication	PES College of Engineering Mandya, Karnataka, INDIA	Mysore University, Karnataka

3. Membership of Professional Bodies:

4. Awards

Award Title	Date of receiving the award	Award issuing authority/ Body / Organization

4. Publications (Journals Conferences)
i. International Journals

Sl. No.	Title of the paper	Name(s) of Author(s)	Name of the Journal	Volume No. Issue No. Year	WOS / Scopus / Both	Impact Factor	Publisher
1	Design and Implementation of 32-Bit High Valency Jackson Adders	Poornima N & V S Kanchana Bhaaskaran	Journal of Circuits, Systems, and Computers (JCSC)	Vol. No.26 Issue No.7	WOS	0.595	WORLD SCIENTIFIC PUBL CO PTE LTD, SINGAPORE

2	Design of Energy Efficient High-Valency Jackson Flagged Adder Architectures	Poornima N & V S Kanchana Bhaaskaran	International Journal of Pure and Applied Mathematics	Vol. No.118 Issue No.22	--		Academic Publications, Kuwait
3	Area Efficient Hybrid Parallel Prefix Adders	Poornima N & V S Kanchana Bhaaskaran	Procedia Materials Science	Vol. No.10	**--**		Elsevier
4	Capacitor Less Low Dropout Voltage Regulator	Poornima N & Sriranganatha Sagar.K.N	International Journal of Electrical and Electronics Engineering (IJEEE)	Vol. No. : 2 Issue : 2,3,4	**--**		
5	FPGA implementation and performance analysis of conventional and modified router design for NOC.	Poornima N & Shivakumar M	International Journal of Information Technology and Computer Engineering (IJITC)	Vol. No. : Issue : Special	**--**		
6	Performance Analysis Of Parallel Prefix Adder	Poornima N & Manjunath Naik V	International Journal of Electrical, Electronics and Data Communication	Vol. No. 3 Issue :7	**--**		
7	IoT BASED GAS LEAKAGE DETECTOR ROBOT	Poornima N & Ashwin M, Chinmaya A, Deepak Bhojani, Harshita Bhojani	International Journal of Research & Technology,	Vol. No. 8 Issue No. 3	--		

ii. International Conferences

Sl. No.	Title of the paper	Name(s) of Author(s)	Name of the Journal	Volume No. Issue No. Year	WOS / Scopus	Impact Factor	Publisher
1	Power-Delay Optimized 32 Bit Radix-4, Sparse-4 Prefix Adder	Poornima N & V S Kanchana Bhaaskaran	Fifth International Conference on Signal and Image Processing (ICSIP), ,2014	doi: 10.1109/ICSIP.2014.38 ISBN: 978-0-7695-5100-5	WOS		IEEE
2	Area Efficient Hybrid Parallel Prefix Adders	Poornima N & V S Kanchana Bhaaskaran	International Conference on Nano materials and Technologies	ISBN:978-81-925751-8-6,	WOS		Elsevier
3	Implementation of Shi-Tomasi Corner	Poornima N & Srividya Krishnapur	National Conference on "Developments in Domain of Electrical	--	--	**--**	--

	Detection Algorithm		Engineering(NCDDEE-2014), SSIT, Tumkur.				
4	FPGA implementation and performance analysis of conventional and modified router design for NOC.	Poornima N & Shivakumar M	4th National Conference on Recent Advances in Science, Engineering & Technology (NCRASET-16) SVCE,B'LORE	--	--	**--**	--

5. Grants/Funding Received

Grant Amount	**Project Name**	Date of receiving the Grant	Grant issuing authority/ Body / Organization
7000	KELLER: Indian Sign Language Gesture to Text and Speech Assistant	23-04-2021	KSCST- 44thSERIES OF STUDENT PROJECT PROGRAMME

6. Others :Workshops / Conference (Orgainsed/Attended)

6.a. Workshops / Conference organized

6.b. Conference Attended (those sponsored by AICTE / ISTE/IETE/TEQIP or any other sponsoring body)

National Workshop on Accreditation Process for Technical Institutions organized by JSSATE Bangalore in association with ISTE,IIIE, QCFI from 26-08-2016 to 27-08-2016
International Conference on Nano materials and Technologies organized by Vardhamaan College of Engineering , Hyderabad sponsored by BARC, Mumbai

6.c. workshop/ Seminar /Conference Attended (those NOT sponsored by AICTE / ISTE/IETE/TEQIP or any other sponsoring body)

AI and ML applications in Image processing using modern tools organized by M S Ramaiah Institute of Technology, Bangalore from 13-07-2020 to 18-07-2020
Machine Learning for All 4 weeks online credit score authorized by University of London and offered through Coursera
Analog and Digital System Design Using CADENCE Tool organized by GSSS Institute of Engineering and Technology, Mysore from 23-01-2019 to 25-01-2019
Signal , Image processing and SDR using Lab View organized by JSSATE Bangalore in association with TECHLABS from 22-06-2015 to 24-06-2015
International conference on Signal and Image processing organized by BNMIT Bangalore from 8-01-2014 to 10-01-2014
National conference on VLSI, Signal and Image processing organized by JSSATE Bangalore from 22-08-2014 to 23-08-2014
Advanced VLSI Design using Cadence Tool Suite organized by Cadence Design Systems India Pvt. Ltd from 16-07-2014 to 18-07- 2014
International conference on VLSI Design Embedded Solutions for Emerging markets-Consumer, Energy, Automotive organized at Hyderabad International Convention Center, Hyderabad from 7-01-2012 to 11-01-2012
National conference on Antennas and its applications organized by VTU, Belguam from 24-02-2012 to 25-02-2012
Advanced trends in Low Power SoC VLSI Design organized by Jain University from 5-10-2012 to 6-10-2012

FPGA Based Embedded System Design organized by JSSATE Bangalore and DEXEL EmDAC on 3-01- 2012
VLSI, MEMS, and Integration organized by VIT, Chennai on 09-10-2011
Analog and Mixed mode Design using Cadence Tool organized by BNMIT Bangalore and CADENCE, Design systems from 2-02-2009 to 4-02-2009
Recent trends in VLSI and Embedded System Design Technology organized by Global Academy of Technology, CADENCE, UTL from 12-04-2007 to 13-04-2007

6.d. PROJECT / Innovations/Patents

6.e. Any other information you will like to share about your professional experience