JSS Mahavidyapeetha
JSS Academy of Technical Education, Bengaluru
Department of Electronics & Communication Engineering

FACULTY PROFILE

1. Personal Details

NAME	Dr. Saroja S Bhusare
DEPARTMENT	Electronics & Communication Engineering
DESIGNATION	Associate Professor
PHONE	+91 9964420351
EMAIL ID	sarojasbhusare@jssateb.ac.in
TEACHING EXPERIENCE	22 Years 3 Months
INDUSTRY EXPERIENCE	-
RESEARCH EXPERIENCE	10 Years

2. Qualification

COURSES	SPECIALIZATION	INSTITUTION	UNIVERSITY
Ph.D	Low Power VLSI	VIT Chennai Tamil Nadu India	School of Electronics and Communication Engineering, VIT Chennai Tamil Nadu India
M.Tech	VLSI Design and Embedded Systems	BMS College of Engineering Bangalore Karnataka INDIA	BMS College of Engineering Bangalore Karnataka INDIA
B.E	Electronics and Communication Engineering	Basaveshwar Engineering College Bagalkot Karnataka INDIA	Karnatak University, Dharwad Karnataka
Diploma	Computer Science and Engineering	B V V S Polytechnic Bagalkot Karnataka INDIA	Board of Technical EXaminatio
SSLC	-	St. Anne's Convent School, Bangalore Karnataka INDIA	Karnataka Secondary Education Examination Board

3. Membership of Professional Bodies:

1. Life Membership in Indian Society for Technical Education (MISTE)

4. Awards

Award Title	Date of receiving the award	Award issuing authority/ Body / Organization
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4. Publications (Journals Conferences)

Sl. No.	Title of the paper	Name(s) of Author(s)	Name of the Journal	Volume No. Issue No. Year	WOS / Scopus / Both	Impact Factor	Publisher
1	Low-Power High-Accuracy Fixed-Width Radix-8 Booth Multiplier Using Probabilistic Estimation Technique	1) Saroja S Bhusare 2) Dr. V S Kanchana Bhaaskaran	Journal of Circuits, systems and computers	Vol. No.26 Issue No.05 pp:1750079 [12 pages] Year:2017	WOS	1.363	World Scientific Publishers
2	High Accuracy Fixed-Width Radix-8 Booth Multiplier Using Adaptive Conditional-Probability Estimator	1) Saroja S Bhusare 2) Dr. V S Kanchana Bhaaskaran	International Journal of Pure and Applied Mathematics	Vol. No.118 Issue No. 26 pp: 1903-1918 Year:2018	Scopus	0.320	Academic Publications
3	A qualitative Analysis of Various Adaptive Routing Algorithms	1)Kavyashree G S 2) Saroja S. Bhusare, 3)Sunita Shirahatti	International Research Journal of Engineering and Technology (IRJET)	Vol. No-03 Issue:05 pp:773-777 Year:2016	**-**	**-**	
4	Design of Pulsed latch Shift Register	1) Veeresh Gavai 2) Veeramma Yatnalli 3) Saroja S Bhusare	International Research Journal of Engineering and Technology (IRJET)	Vol. No-05 Issue:05 pp:2766-2769 Year:2017	-	**-**	
5	Implementation of IoT based Smart Village for the Rural Development	1)Medara Sahana 2)Yarraguntla Sarala 3)Anushka Bisht 4) Pavitra Bhovi 5) Dr. Saroja S Bhusare	International Journal of Research and Technology	Vol. No-08 Issue:03 Year:2020	**-**	**-**	**-**
6	Review of IoT based Smart Village for the Rural Development	1)Medara Sahana 2)Yarraguntla Sarala 3)Anushka Bisht 4) Pavitra Bhovi 5) Dr. Saroja S Bhusare	International Journal of Engineering Research & Technology (IJERT)	Vol. No-08 Issue:04 Year:2020	**-**	**-**	**-**
7	Wheelchair Control Using Brain Computer Interface	1) Veeramma Yatnalli 2) B G Shivaleelavati 3) Saroja S Bhusare	International Journal of Future Generation Communication and Networking, Science & Engineering	Vol. 14 No. 1 Year 2021	WOS	0.4	Science & Engineering Research Support society
8	Fixed-Width Multiplier with Simple Compensation Bias	1) Saroja S Bhusare 2) Dr. V S Kanchana Bhaaskaran	Procedia Material Science	Vol. No.10 pp:395-402 Year:2015	WOS	-	Science Direct

Conferences

Sl. No.	Title of the paper	Name(s) of Author(s)	Name of the Journal	Volume No. Issue No. Year	WOS / Scopus	Impact Factor	Publisher
1	Design and FPGA Implementation of Improved Lifting Scheme based DWT for OFDM Systems	1)H S Deepthi 2) Sumita Shankar Manure 3) Cyril Prasanna Raj P 4) Saroja S Bhusare 5)U L Naik	3RD International Conference on Advances in Recent Technologies in Communication and Computing ARTcomm 2011	pp 184-127 Year 2011	-	**-**	IET (IET Digital Library)
2	Low Power ASIC Implementation of a 256 Bit Key AES Crypto-Processor at 45nm Technology	1)Ashwin R 2)Saroja S Bhusare	International Conference on Electronics and Electrical Engineering ICEEE-2012 30th june 2012 organized by IOJA at Mysore India	Year 2012	-		IPM Pvt. Ltd
3	Design, Analysis and Simulation of Self Bias Phase Lock Loop with Different Locking Techniques	1) Divyashree S 2) Saroja S Bhusare	International Conference on Electronics and Electrical Engineering ICEEE-2012 30th june 2012 organized by IOJA at Mysore India	Year 2012			IPM Pvt. Ltd
4	Design of a Low Error Fixed-Width Radix-8 Booth Multiplier	1) Saroja S Bhusare 2) Dr. V S Kanchana Bhaaskaran	Signal and Image Processing (ICSIP), 2014 Fifth International Conference on Signal and Image Processing	pp:206-209 Year:2014	Yes		IEEE Xplore
5	Architectural based congestion management for Network on Chip implemented on FPGA	1)Kavyashree G S 2) Saroja S. Bhusare 3)Sunita Shirahatti	2nd International Conference on Applied and Theoretical Computing and Communication Technology (iCATccT), 2016 IEEE	pp:256-261 Year-2016	Yes		IEEE Xplore
6	Review of IoT based Smart Village for Rural Development	1)Medara Sahana 2)Yarraguntla Sarala 3)Anushka Bisht 4) Pavitra Bhovi 5) Saroja S Bhusare	1st National Conference on Emerging Trends in Engineering Science for Future Technology	Vol. No-08 Issue:14 pp 195-203 Year 2020 **Selected as best Paper**	**-**		International Research Publication House
7	Wheelchair Control Using Brain Computer Interface	1) Veeramma Yatnalli 2) B G Shivaleelavati 3) Saroja S Bhusare	National Conference on Bioengineering, Biotechnology and Medical Engineering Dept., NIT, Rourkela, India	Abstract Presentation 10th-11th December 2020			
8	Smart Health Care and Tracking System Based on Internet of Things	1) B G Shivaleelavati 2) Veeramma Yatnalli 3) Saroja S Bhusare	National Conference on Bioengineering, Biotechnology and Medical Engineering Dept., NIT, Rourkela, India	Abstract Presentation 10th-11th December 2020			

6. Grants/Funding Received

Grant Amount	**Project Name**	Date of receiving the Grant	Grant issuing authority/ Body / Organization
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6.Others :Workshops / Conference (Orgainsed/Attended)

6.a. Workshops / Conference organized

National Conference on VLSI, Signal and Image Processing, JSS Academy of Technical Education, Bangalore, 22-08-14 to 23-08-14, Organizing Committee Member
Signal, Image Processing and SDR Using LABVIEW, JSS Academy of Technical Education, Bangalore in Association with Techlabs, 22-06-15 to 24-06-15, Organizing Committee Member
Design Verification using Verilog and System Verilog, JSS Academy of Technical Education, Bangalore in association with EDULIFE INDIA, 26-11-15 to 27-11-15, Organizing Committee Member

6.b. Conference Attended (those sponsored by AICTE / ISTE/IETE/TEQIP or anyother sponsoring body)

Digital Signal Processing and Applications, Department of Electronics and Computer Science Engineering, Bangalore University, Bangalore Bangalore and AICTE Delhi, 29-07-02 to 14-08-02
Accreditation Process for Technical Institutions, JSS Academy of Technical Education, Bangalore in Association with VTU, ISTE, IIIE and QCFI, 26-08-16 to 27-08-16

6.c. workshop/ Seminar /Conference Attended (those NOT sponsored by AICTE / ISTE/IETE/TEQIP or anyother sponsoring body)

Mixed-Signal VLSI, Bangalore Institute of Technology, Bangalore, 18-02-2005 to 23-02-2005
A Short term Course on System C, JSS Academy of Technical Education, Bangalore, 06-04-05 to 08-04-05
Cadence Tools Training, Cadence, Bangalore, 03-03-06
VLSI Design using Cadence Tools, Sri Venkateshwara College of Engineering, Bangalore, 27-02-06 to 02-03-06
Recent Trends in VLSI and Embedded System Design Technology, Global Academy of Technology, Bangalore, 12-04-07 to 13-04-07
Cadence Tools Training, Cadence, Bangalore, 20-09-07
Cadence Tools Training, , Cadence, Bangalore, 14-03-08
Analog and Mixed-mode Design using Cadence Tool, B N M Institute of Technology, Bangalore, 02-02-09 to 04-02-09
VLSI, MEMS and Integration, SENSE, VIT Chennai, 09-12-11 to 10-12-11
FPGA based Embedded System Design, JSS Academy of Technical Education, Bangalore in Collaboration with Dexcel-EmDAC, 03-01-12
25th International Conference on VLSI Design, Hyderabad, 07-01-12 to 11-01-12
Advanced Trends in Low Power SoC VLSI Design, Center for Emerging Technologies, Jain University, Bangalore, 05-10-12 to 06-10-12
National Conference on Antennas and Applications, Regional Campus, VTU, Bangalore, 24-02-12 to 25-02-12
International Conference on Electrical and Electronics Engineering, Mysore, 30-06-12
Fifth International Conference on Signal and Image Processing, BNM Institute of Technology, Bangalore, 8-01-14 to 10-01-14
Advanced VLSI Design using Cadence Tool Suite, JSS Academy of Technical Education in Association with Cadence Design Systems India Pvt. Ltd., Bangalore, 16-07-14 to 18-07-14
2ND International Conference on Nanomaterials and Technologies CNT-1014, Vardhaman College of Engineering, Hyderabad, 17-10-14 to 18-10-14
Design Verification using Verilog and System Verilog, JSS Academy of Technical Education, Bangalore in association with EDULIFE INDIA, 26-11-15 to 27-11-15
GNU Radio and Software Defined Radio, JSS Academy of Technical Education, Bangalore in Association with Tenet Technetronics, 27-06-16 to 01-07-16
Advances in VLSI Design AVLSID-2017, Bangalore Institute of Technology, Bangalore, 03-04-17 to 05-04-17
National Symposium on Internet of Things-Trends and Opportunities, Centre for Interdisciplinary Research, JSS Academy of Technical Education, Bangalore, 04-07-18 to 05-07-18
AI and ML Applications in image processing using modern tools, Ramaiah Institute of technology, Bangalore, 13-07-2020 to 18-07-2020

6.d. PROJECT / Innovations/Patents

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6.e. Any other information you will like to share about your professional experience