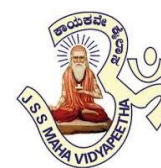





**JSS Mahavidyapeetha**  
**JSS Academy of Technical Education, Bengaluru**  
**Department of Electronics & Communication Engineering**



**FACULTY PROFILE**

**1. Personal Details**

NAME	Kavitha M	
DEPARTMENT	Electronics & Communication Engineering	
DESIGNATION	Assistant Professor	
PHONE	9449238353	
EMAIL ID	mkavitha@jssateb.ac.in	
TEACHING EXPERIENCE	20 Years	
INDUSTRY EXPERIENCE	Nil	
RESEARCH EXPERIENCE	5 Years	

**2. Qualification**

COURSES	SPECIALIZATION	INSTITUTION	UNIVERSITY
ATS or any other certification	VLSI Design & Embedded Systems	BMSCE, Bangalore	VTU
BE / Diploma / ITI	Electronics & Communication Engineering	MVIT, Bangalore	Bangalore
PUC	PCMB	JNV, Mandya	CBSE
SSLC	X Standard	JNV, Mandya	CBSE

**3. Membership of Professional Bodies:**

1. <b>Example : 1. Life Membership in Indian Society for Technical Education ( MISTE)</b>
2.

**4. Awards**

Award Title	Date of receiving the award	Award issuing authority/ Body / Organization

**5. Publications ( Journals Conferences )**

Sl. No	Title of the paper	Name(s) of Author(s)	Name of the Journal	Volume No. Issue No. Year	WOS / Scopus / Both	Impact Factor	Publisher
1	<b>Analysis and Design of different OTA topologies for Bio-potential signals</b>	Kavitha M, Dr S Akhila	International Journal of future generation and communication Networking	Vol.14,No.1,2021	WoS	0.41	SERSC
2	Design and Performance analysis of a Low Power First order sigma Delta modulator	Kavitha M, Dr. H B Bhuvaneshwari	International Journal of Applied Engineering Research	Online ISSN : 0973-4562 Volume No. : 10 Issue No. : 92 Month & Year : 2015 Page Nos. : 284-290	Scopus	0.14	
3	An 8-bit area optimized low power continuous time band pass sigma-delta ADC in 45nm CMOS	Kavitha M, Rahul	International Journal of Information Technology and Computer Engineering	Online ISSN : 2319-6890 Volume No. : 4 Issue No. : 3 Month & Year : May 2015 Page Nos. : 155-159			
4	FPGA Implementation of Four-Channel Bit Error Rate Tester for Spacecraft Data Acquisition System	Kavitha M, Sinchana	International Journal of Information Technology and Computer Engineering	e- ISSN : 2455-529 Month & Year : 2016 Page Nos. : 109-113			

#### 6. Grants/Funding Received

Grant Amount	Project Name	Date of receiving the Grant	Grant issuing authority/ Body / Organization

**6.Others :Workshops / Conference (Orgained/Attended)**

**6.a. Workshops / Conference organized**

Sl. No.	Title of the paper	Name(s) of Author(s)	Name of the Conference	Volume No. Issue No. Year	WOS / Scopus	Impact Factor	Publisher
1	Switched Capacitor Implementation of First Order Sigma-Delta Modulator	Kavitha M, Dr S Akhila	2018Third International Conference Electrical, Electronics Communication, Computer Technologies and Optimization Techniques (ICEECCOT)14-15, December 2018				
2	FPGA Implementation of Four-Channel Bit Error Rate Tester for Spacecraft Data Acquisition System	Kavitha M, Sinchana	4 <sup>th</sup> National Conference on “Recent Advances in Science, Engineering and Technology (NCRASET-16)” organized by Sri Venkateshwara College of Engineering, Bangalore.				
3	An 8-bit area optimized low power continuous time band pass sigma-delta ADC in 45nm CMOS	Kavitha M, Rahul	2 <sup>nd</sup> International Conference on Convergent innovative Technologies ICCIT-2015 held at Cambridge Institute of Technology, Bangalore				
4	FPGA implementation 4-channel bit error rate tester for space trak data aquasition system	Kavitha M, Madhusudhan	NCRASET-16				

**6.b. Conference Attended ( those sponsored by AICTE / ISTE/IETE/TEQIP or anyother sponsoring body)**


**6.c. workshop/ Seminar /Conference Attended ( those NOT sponsored by AICTE / ISTE/IETE/TEQIP or anyother sponsoring body)**

<b>Sl. No.</b>	<b>Name of the workshop / Conference</b>	<b>Organiser</b>	<b>Date</b>
1	Six days short term programming programme on Industry 4.0 sponsored by AICTE	Department of Electronics and Communication Engineering, ACSCE, Bangalore	9 <sup>th</sup> to 14 <sup>th</sup> November 2020
2	AI and ML applications in Image processing using modern tools	M S Ramaiah Institute of technology, Bangalore	13 <sup>th</sup> to 18 <sup>th</sup> July 2020
3	Three Day Faculty Development Program on “Analog and Digital System Design using Cadence Tool”	Department of Electronics and Communication Engineering, GSSSIETW, Mysore	23 <sup>rd</sup> to 25 <sup>th</sup> January 2019
4	5 Days Faculty Development Program on “GNU Radio and Software Defined Radio”	Department of Electronics & Communication Engineering at JSSATE, Bangalore.	27 <sup>th</sup> June 2016 to 1 <sup>st</sup> July 2016
5	one week workshop on “Electronics System Design, Manufacturing & Testing(ESDMT)”	Department of Electronics & Instrumentation Engineering at BMSCE, Bangalore in association with Entuple Technologies.	27 <sup>th</sup> to 31 <sup>st</sup> July 2015
6	Didactic Seminar on “Cadence OrCAD PSPICE and ORCAD PCB”.	Department of Electronics & Instrumentation Engineering at BMSCE, Bangalore	31 <sup>st</sup> July 2015
7	workshop on “Signal, Image	Department of	22 <sup>nd</sup> to 24 <sup>th</sup> June 2015

	Processing and SDR using LabView”.	Electronics & Communication Engineering at JSSATE, Bangalore.	
8	3 day Faculty Development Program on “Advanced VLSI Design using Cadence Tool Suite”	Department of Electronics & Communication Engineering at JSSATE, Bangalore.	16 <sup>th</sup> , 17 <sup>th</sup> & 18 <sup>th</sup> July 2014
9	5 day Hands-on workshop on “Analog & Digital Chip Design Using Cadence”.	Department of Electronics & Communication Engineering at Nitte Meenakshi Institute of Technology, Bangalore	22 <sup>nd</sup> to 26 <sup>th</sup> July 2014
10	Participated as a Delegate in the 26 <sup>th</sup> Indian Engineering Congress.	Organized by Indian Engineering Congress, Bangalore.	15 <sup>th</sup> to 18 <sup>th</sup> December 2011


**6.d. PROJECT / Innovations/Patents**


**6.e. Any other information you will like to share about your professional experience**